What is claimed is:

(Claim 1) 1. A receiver system processing an input signal containing signals of interest and unwanted interference signals, wherein said signals of interest are present in a frequency band of interest, said input signal being formed using a carrier frequency, said receiver system comprising:

a mixer processing said input signal to generate an intermediate signal in the form of electric current, wherein said intermediate signal is generated with said frequency band of interest centered at a first frequency not equal to said carrier frequency; and

a filter circuit filtering said unwanted interference signals from said intermediate signal received in the form of electric current to generate said signals of interest as an output signal.

(Claim 2) 2. The receiver system of claim 1, wherein said output signal is generated in the form of electric voltage, said receiver system further comprising an analog to digital converter (ADC) converting said output signal in the form of electric voltage to a plurality of digital codes representing said signals of interest.

(Claim 3) 3. The receiver system of claim 2, further comprising a low noise amplifier which provides said input signal in an amplified form to said mixer.

(Claim 4) 4. The receiver system of claim 1, wherein said first frequency is lower than said carrier frequency.

(Claim 5) 5. The receiver system of claim 4, wherein said first frequency equals 0.

(Claim 6) 6. The receiver system of claim 1, wherein said mixer is implemented with a high gain to generate said intermediate signal with a larger swing of electric current compared to the swing of electric voltage in response to changes in input signal.

(Claim 7) 7. The receiver system of claim 6, wherein said filter circuit is implemented with low input impedance to receive said electric current.

(Claim 8) 8. The receiver system of claim 1, wherein said mixer comprises:

a first transistor, a second transistor and a third transistor, each comprising a source terminal, a drain terminal and a gate terminal; and

a first current source and a second current source together setting a bias point for linear operation of each of said first transistor, said second transistor and said third transistor,

wherein one terminal of each of said first current source and said second current source is connected to a supply voltage, the other terminal of said first current source being connected to the drain terminal of said second transistor at a first node, the other terminal of said second current source being connected to the drain terminal of said third transistor,

the gate terminal of said each of said second transistor and said third transistor being connected to receive a fixed frequency signal,

the source terminals of said second transistor and said third transistor being connected to the drain terminal of said first transistor,

the source terminal of said first transistor being connected to Vss, and

the gate terminal of said first transistor being connected to receive said input signal.

(Claim 9) 9. The receiver system of claim 8, wherein each of said first transistor, said second transistor and said third transistor comprises a NMOS transistor.

(Claim 10) 10. The receiver system of claim 8, wherein said filter circuit is implemented as a first order filter.

(Claim 11) 11. The receiver system of claim 10, wherein said filter circuit comprises:

an operational amplifier having an inverting terminal and a non-inverting terminal, said inverting terminal being connected to said first node; and

a resistor and a capacitor connected in parallel between said inverting terminal and an output terminal of said operational amplifier.

(Claim 12) 12. The receiver system of claim 11, wherein said inverting terminal is connected to said first node without a resistor in between.

(Claim 13) 13. The receiver system of claim 8, wherein said filter circuit is implemented as a second order filter.

(Claim 14) 14. The receiver system of claim 13, wherein said filter circuit comprises:

a first resistor having one terminal connected to said first node;

a first capacitor being connected between said one terminal of said first resistor and Vss;

an operational amplifier having an inverting terminal and a non-inverting terminal, said inverting terminal being connected to another terminal of said first resistor;

a second resistor connected between said first node and an output terminal of said operational amplifier; and

a second capacitor connected between said inverting terminal and said output terminal.

(Claim 15) 15. The invention of claim 1, wherein said receiver system is comprised in a Wireless Local Area Network (WLAN) receiver.

(Claim 16) 16. A receiver system processing an input signal containing signals of interest and unwanted interference signals, wherein said signals of interest are present in a frequency band of interest, said input signal being formed using a carrier frequency, said receiver system comprising:

means for converting said input signal to an intermediate signal in the form of electric current, wherein said intermediate signal is generated with said frequency band of interest centered at a first frequency not equal to said carrier frequency; and

means for filtering said unwanted interference signals from said intermediate signal received in the form of electric current to generate said signals of interest as an output signal.

(Claim 17) 17. The receiver system of claim 16, wherein said means for filtering amplifies said signals of interest and provides said output signal in a voltage domain.

(Claim 18) 18. A method of processing an input signal containing signals of interest and unwanted interference signals, wherein said signals of interest are present in a frequency band of interest, said input signal being formed using a carrier frequency, said method comprising:

converting said input signal to an intermediate signal in the form of electric current, wherein said intermediate signal is generated with said frequency band of interest centered at a first frequency not equal to said carrier frequency; and

filtering said unwanted interference signals from said intermediate signal received in the form of electric current to generate said signals of interest as an output signal.

(Claim 19) 19. The method of claim 18, wherein said output signal is provided in a voltage domain.

(Claim 20) 20. The method of claim 19, further comprising sampling said output signal in said voltage domain.